What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate which has a major surface;

a MOS transistor which has a gate and first and second diffusion regions and which is formed on the major surface; and

a laminated structure of a SOG layer, said laminated structure being composed of a base layer and a surface layer formed on the base layer and being formed over said MOS transistor; the surface layer being denser than the base layer.

2. A semiconductor device as set forth claim 1, wherein the laminated structure has a first contact hole defined therein, the first contact hole exposing the first diffusion region of said MOS transistor; and

a first conductive material formed within the first contact hole.

3. A semiconductor device as set forth claim 2, wherein the first diffusion region is a source or a drain of said MOS transistor.

4. A semiconductor device as set forth claim 2, further comprising;

said laminated structure has a second contact hole defined therein, the second contact hole exposing the second diffusion region of said MOS transistor.; and

a second conductive material formed within the second contact hole.

5. A semiconductor device as set forth claim 4, wherein the second diffusion region is a source or a drain of said MOS transistor.

6. A semiconductor device as set forth claim 5, wherein the first conductive material is a bit line and the second conductive material is an electrode of a capacitor.

7. A method of fabricating a semiconductor device comprising:

forming a SOG layer over a MOS transistor formed on a semiconductor substrate;

converting a surface portion of the SOG layer into to a dense layer which is denser than a bottom portion of the SOG layer;

removing a first portion of the dense layer to expose a surface of the bottom portion of the SOG layer by a first etching;

removing a second portion which corresponds to the exposed surface of the bottom portion of the SOG layer to expose a diffusion region of the MOS transistor by a second etching; and

forming a conductive material within a space in which the first and second portions are removed.

8. A method of fabricating a semiconductor device as set forth claim 7, wherein said converting step comprises implanting ions into the surface portion of the SOG layer.

9. A method of fabricating a semiconductor device as set forth claim 7, wherein the first etching is an anisotropic etching and the second etching is an isotropic etching.

10. A semiconductor device comprising:

a semiconductor substrate which has first and second regions formed on a major surface thereof;

a first insulating layer which is formed over the first region;

a dummy pattern which has a predetermined shape and which is formed on said first insulating layer;

a first SOG layer which is formed on side surfaces of said dummy pattern and the first insulating layer;

a second SOG layer which is formed on a top surface of said dummy pattern and said first SOG layer, said second SOG layer being denser than said first SOG layer; and

a second insulating layer which is formed on said second SOG layer,

wherein said first and second insulating layers and said first and second SOG layers are exposed at a boundary between the first region and the second region.

11. A semiconductor device as set forth claim 10, wherein the second region is a grid line.

12. A semiconductor device as set forth claim 10, further comprising a fuse element which is formed over the second region.

13. A semiconductor device comprising:

a semiconductor substrate which has first and second regions formed on a major surface thereof, the second region surrounding the first region;

a first insulating layer which is formed over the second region;

a dummy pattern which has a frame shape surrounding the first region and which is formed on said first insulating layer;

a first SOG layer which is formed on side surfaces of said dummy pattern and the first insulating layer;

a second SOG layer which is formed on a top surface of said dummy pattern and said first SOG layer, said second SOG layer being denser than said first SOG layer; and

a second insulating layer which is formed on said second SOG layer,

wherein said first and second insulating layers and said first and second SOG layers are exposed at a boundary between the first region and the second region.

14. A semiconductor device as set forth claim 13, further comprising a fuse element which is formed over the first region.

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